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EXAMINER	
CHRISS, ANDREW W	

ART UNIT	PAPER NUMBER
2472	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,665	DIEHL ET AL.	
	Examiner	Art Unit	
	ANDREW CHRISS	2472	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-14,20-24 and 28-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-14, 20-24 and 28-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment, filed May 10, 2010, has been entered and carefully considered. Claim 1 is amended, Claims 5-8, 15-19, and 25-27 are canceled, Claims 29-32 are newly added, and Claims 1-4, 9-14, 20-24, and 28 are currently pending.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 1-3, 9-13, 20-24, and 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski et al (United States Patent 6,265,894), hereinafter Reblewski, in view of Kappler et al (United States Patent 6,064,677), hereinafter Kappler, and Duan et al (United States Patent 5,923,656), hereinafter Duan.

Regarding Claims 1 and 9, Reblewski teaches a reconfigurable integrated circuit for use in an emulation system (column 1, line 66 – column 2, line 2). However, Reblewski does not teach a storage unit comprising a signal inclusion schedule or circuitry operative to generate and transmit a message. In the same field of endeavor, Kappler teaches a calendar queue mechanism for scheduling transport of units or cells, specifically high frequency/high priority flows and low frequency/low priority flows (column 12, line 65 – column 13, line 10). Further, Kappler teaches a set of transmit lists 65, connected to calendar queue 63 (Figure 3), which generate and transmit the messages released by the calendar queue (column 11, lines 25-30). As mentioned above, the calendar queue specifies the frequency of the signals to include. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms. However, the aforementioned references do not disclose selecting a plurality of signals from at least one pin. In the same field of endeavor, Duan discloses a cell scheduler in an ATM switch fabric that selects a "winning" set of cells (i.e., plurality of signals) from multiple FIFO rooms in a memory (Figure 2; column 7, lines 17-35 and 53-64). Although Duan does not explicitly disclose selecting the signal from a pin, it would have been obvious to one of ordinary skill in the art that the selection of a cell for transfer would comprise transmission over an IC pin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduler disclosed in Duan with the reconfigurable integrated disclosed in Reblewski, as modified above, in order to maximize transmission opportunities for available ports in an ATM switch fabric (see column 3, lines 18-29 of Duan).

Regarding Claims 2 and 10, Reblewski does not teach signals determined to be more critical transmitted more frequently. In the same field of endeavor, Kappler further teaches flows having different frequencies are prioritized so that the data transport units of the higher frequency flows are given transmit priority over any data transport units of lower frequency flows with which they happen to collide (column 12, lines 30-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in

Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 3 and 12, Reblewski does not teach generating and transmitting a message in a plurality of clock cycles of an operating clock independent of an emulation clock. In the same field of endeavor, Kappler further teaches that the calendar queue 63 implements a stalled virtual clock so that cells that are scheduled for transmission are leased for transmission only when system "real time" has reached their respective scheduled transmission times (column 11, lines 21-25). Therefore, messages are generated in a plurality of clock cycles of an operating clock independent of the predetermined rate of the overall system clock (column 8, lines 53-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 11, Reblewski does not teach the message comprising state values. In the same field of endeavor, Kappler teaches that each outbound message contain VP and VC identifiers (Figure 2), equivalent to Applicant's disclosed state value (Figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 13, Reblewski does not teach extracting a parity value from a message. In the same field of endeavor, Kappler teaches reading a CRC (parity) value from an inbound cell (Figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 20, Reblewski teaches an integrated circuit for use in an emulation system, as described with regards to Claims 1 and 9. Reblewski further teaches multiple reconfigurable logic resources (Figure 2), output pins 113, and a partial scan register that receives a plurality of output signals from logic elements (column lines 6-15), equivalent to Applicant's claimed message formation and send block. However, Reblewski does not teach a signal inclusion schedule. In the same field of endeavor, Kappler teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms. However, the aforementioned references do not disclose selecting a plurality of signals from at least one pin. In the same field of endeavor, Duan discloses a cell scheduler in an ATM switch fabric that selects a "winning" set of cells (i.e., plurality of signals) from multiple FIFO rooms in a memory (Figure 2; column 7, lines 17-35 and 53-64). Although Duan does not explicitly disclose selecting the signal from a pin, it would have

been obvious to one of ordinary skill in the art that the selection of a cell for transfer would comprise transmission over an IC pin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduler disclosed in Duan with the reconfigurable integrated disclosed in Reblewski, as modified above, in order to maximize transmission opportunities for available ports in an ATM switch fabric (see column 3, lines 18-29 of Duan).

Regarding Claim 21, Reblewski teaches an input pin 113. Reblewski further teaches a logic element that receives multiple inputs and outputs a single signal (truth table 202). However, Reblewski does not teach the claimed message receive and disassembly block nor the signal inclusion schedule. In the same field of endeavor, Kappler teaches a switching fabric that decomposes cells into four bit wide "nibbles" for arbitration and routing (column 10, lines 7-13), equivalent to Applicant's claimed message received and disassembly block. Kappler further teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 22, Reblewski teaches a plurality of output pins 113. Further, Reblewski teaches an array of reconfigurable integrated circuits in Figure 10, thereby teaching multiple partial scan registers.

Regarding Claim 23, Reblewski teaches an array of reconfigurable integrated circuits in Figure 10, thereby teaching a plurality of reconfigurable logic resources in communication with the message formation and send block.

Regarding Claim 24, Reblewski teaches an integrated circuit for use in an emulation system, as described with regards to Claims 1, 9, and 20. Reblewski further teaches multiple reconfigurable logic resources (Figure 2) and input pins 113. However, Reblewski does not teach the claimed message receive and disassembly block nor the signal inclusion schedule. In the same field of endeavor, Kappler teaches a switching fabric that decomposes cells into four bit wide "nibbles" for arbitration and routing (column 10, lines 7-13), equivalent to Applicant's claimed message received and disassembly block. Kappler further teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms. However, the aforementioned references do not disclose selecting a plurality of signals from at least one pin. In the same field of endeavor, Duan discloses a cell scheduler in an ATM switch fabric that selects a "winning" set of cells (i.e., plurality of signals) from multiple FIFO rooms in a memory (Figure 2; column 7, lines 17-35 and 53-64). Although Duan does not explicitly disclose selecting the signal from a pin, it would have been obvious to one of ordinary skill in the art that the selection of a cell for transfer would comprise transmission over an IC pin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduler disclosed in Duan with the

reconfigurable integrated disclosed in Reblewski, as modified above, in order to maximize transmission opportunities for available ports in an ATM switch fabric (see column 3, lines 18-29 of Duan).

Regarding Claim 32, Reblewski does not disclose the order specified by the signal inclusion schedule is determined based on the determined frequency of occurrence. In the same field of endeavor, Kappler teaches a calendar queue mechanism for scheduling transport of units or cells, specifically high frequency/high priority flows and low frequency/low priority flows (column 12, line 65 – column 13, line 10). Further, Kappler teaches a set of transmit lists 65, connected to calendar queue 63 (Figure 3), which generate and transmit the messages released by the calendar queue (column 11, lines 25-30). As mentioned above, the calendar queue specifies the frequency of the signals to include. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

4. **Claims 4 and 14** rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski in view of Kappler and Duan as applied to claims 1 and 13 above, and further in view of Sindhushayana et al (United States Patent Application Publication US 2003/0053435 A1), hereinafter Sindhushayana. Reblewski, Kappler, and Duan teach all of the limitations of Claims 1 and 13, as discussed above. However, the references do not teach a parity bit generator. In the same field of endeavor, Sindhushayana teaches a channel interleaver that permutes systematic bits with parity bits, thus generating a parity value and transmitting a message containing a parity

value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the parity value generator taught in Sindhushayana with the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to employ an error correction system that overcomes the impact of interference in a wireless system.

5. **Claim 28** rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski in view of Kappler and Duan as applied to Claim 24 above, and further in view of Parruck et al (United States Patent 6,198,723), hereinafter Parruck. The combination of Reblewski, Kappler, and Duan discloses all of the limitations of Claim 24, as described above. However, the aforementioned references do not disclose different signal inclusion schedules. In the same field of endeavor, Parruck discloses a traffic shaping device using multiple round robin schedulers (Figure 4, 212; column 7, lines 61-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multiple schedulers disclosed in Parruck with the reconfigurable IC disclosed in Reblewski, as modified above, in order to shape output traffic and meet quality of service criteria.

6. **Claim 29** is rejected under 35 U.S.C. 103(a) as being unpatentable over Rebelwski in view of Kappler and Duan as applied to claim 1 above, and further in view of Ofek (United States Patent 6,731,638). The combination of Reblewski, Kappler, and Duan discloses all of the limitations of Claim 1, as described above. However, the above references do not disclose a message send schedule and a message receive schedule. In the same field of endeavor, Ofek discloses a switch scheduling controller that receives input schedule request messages, maintains a schedule of all possible time slots for each input port and each output port (i.e., message receive and message send schedules) (Figure 22; column 21, lines 1-30). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduling disclosed in Ofek with the reconfigurable IC disclosed in Reblewski, as modified above, in order to maintain a common time reference between all switches deployed in a network (see column 5, lines 15-25 of Ofek).

7. **Claims 30 and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rebelwski in view of Kappler and Duan as applied to claim 1 above, and further in view of Shah et al (United States Patent Application Publication US 2003/0099242).

Regarding Claim 30, the combination of Reblewski, Kappler, and Duan discloses all of the limitations of Claim 1, as described above. However, the above references do not disclose transmitting a message for a number of clock cycles and determining a signal inclusion schedule to provide a number of signal selections equal to the number of clock cycles. In the same field of endeavor, Shah discloses transmission of a cell within K clock cycles, wherein integer K is the number of cycles that the scheduler can finish payload scheduling (paragraph 0067). Examiner submits that because the disclosed variable K is an integer, the value of K could be equal to 1; therefore, the claim limitation of providing a number of signal selections (i.e., cell transmission) equal to the number of clock cycles is met by the disclosure of Shah. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cell scheduling disclosed in Shah with the reconfigurable IC disclosed in Reblewski, as modified above, in order to increase the amount of bandwidth supported by a switching fabric (see paragraphs 0004-0005 of Shah).

Regarding Claim 31, the combination of Reblewski, Kappler, and Duan discloses all of the limitations of Claim 1, as described above. However, the above references do not disclose

transmitting a message for a number of clock cycles and determining a signal inclusion schedule to provide a number of signal selections less than the number of clock cycles. In the same field of endeavor, Shah discloses transmission of a cell within K clock cycles, wherein integer K is the number of cycles that the scheduler can finish payload scheduling (paragraph 0067). Examiner submits that because the disclosed variable K is an integer, the value of K could be a value greater than the number of cells transmitted; therefore, the claim limitation of providing a number of signal selections (i.e., cell transmission) less than the number of clock cycles is met by the disclosure of Shah. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cell scheduling disclosed in Shah with the reconfigurable IC disclosed in Reblewski, as modified above, in order to increase the amount of bandwidth supported by a switching fabric (see paragraphs 0004-0005 of Shah).

Response to Arguments

8. Applicant's arguments, filed May 10, 2010, with respect to rejections of Claim 28 under 35 U.S.C. 112, first paragraph, have been fully considered and are persuasive. The rejections of Claim 28 under 35 U.S.C. 112, first paragraph, have been withdrawn.

9. Applicant's arguments filed May 10, 2010 regarding rejection of Claims 1, 9, 20, and 24 under 35 U.S.C. 103(a) have been fully considered but they are not persuasive. Examiner notes that Applicant has adequately traversed the assertion of Official Notice in the Office Action mailed November 10, 2009. Per MPEP 2144.03: "If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 CFR 1.104(c)(2). See also *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697 ("[T]he Board [or examiner] must point to some concrete

evidence in the record in support of these findings" to satisfy the substantial evidence test)." Examiner submits the following documentary evidence to support the assertion of Official Notice regarding the transmission over an IC pin in an ATM switch. Parry (United States Patent 5,406,554) discloses FIFOs embodied on integrated circuits (column 1, lines 20-48; column 4, line 49 – column 5, line 6) utilized in an ATM switch in order to reassemble messages (Figures 1, 3, and 4; column 14, lines 15-30). Buhrgard et al (United States Patent 5,604,739) discloses an ATM switch circuit architecture comprising conductors and buses connecting respective boards via pin connectors (column 6, lines 45-50) and integrated circuits performing multiplexing/demultiplexing operations (column 7, lines 15-20). Ganmukhi et al (United States Patent 5,541,918) discloses an ATM switch embodied on an integrated circuit providing high speed ATM cell input and output with the ATM network external to the integrated circuit device (column 1, line 63 – column 2, line 10). Examiner submits that the above-cited references show that ATM switches performing messaging processing and reassembly comprise integrated circuits with pins/outputs are well known in the art, and as such, constitute sufficient documentary evidence to support the assertion of Official Notice. Therefore, rejection of Claims 1, 9, 20, and 24 under 35 U.S.C. 103(a) is maintained.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDREW CHRISS whose telephone number is (571)272-1774. The examiner can normally be reached on Monday - Friday, 7:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Chriss
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7/16/2010

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